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A Statistical Approach to the Design of Diffused Junction Transistors

Abstract: Monte Carlo methods of statistical analysis are applied to the problems of transistor design and optimization. The experimental tolerances associated with any diffusion process are shown to represent an important factor in the initial design of diffused junction transistors. Many transistor parameters exhibit a substantial degree of sensitivity to small variations in the diffusion process. This is confirmed by a comparison between the theoretical and experimental open-base breakdown voltage, and current gain, for a large number of devices. It is therefore proposed that the design of a transistor be based upon attaining a specified set of electrical characteristics when the device is assumed to be fabricated by a non-ideal diffusion process. An electronic computer has been used in an investigation of the foregoing problem. The investigation shows further that a margin-of-safety must be designed into each electrical parameter of a transistor to assure that the resulting device satisfies a given set of design specifications, even though this margin-of-safety may differ for each parameter. In this paper examples are presented to illustrate the theoretical trade-off between several opposing transistor parameters that exhibit a substantial degree of variability due to a non-ideal diffusion process.

Symbols

B	Base region transport ratio	BV_{CEO}	Open-base breakdown voltage
$C(x)$	Impurity atom density distribution	V_{PTC}	Collector junction punch-through voltage
C_b	Bulk impurity atom density in semiconductor	V_{PTE}	Emitter junction punch-through voltage
C_c	Collector junction capacitance	V_T	Total junction voltage
C_e	Emitter junction capacitance	W_e	Electrical base width—see Fig. 1
C_{oi}	Impurity atom surface concentration	W_p	Physical base width—see Fig. 1
D_i	Impurity atom diffusion constant	a, b	Constants
ΔH_i	Impurity atom activation energy in silicon	k	Boltzmann's constant
L_n	Minority carrier diffusion length for electrons	q	Electron charge
L_p	Minority carrier diffusion length for holes	t_n	Impurity atom diffusion time
M	Carrier multiplication in collector space-charge layer	x_n	Junction space-charge layer edges—see Fig. 1
P	Arbitrary parameter magnitude	x_{ie}	Emitter junction transition point—see Fig. 1
ΔP	Arbitrary parameter range of variability	x_{ic}	Collector junction transition point—see Fig. 1
R	Gas constant	β_B	Base region transport efficiency $B/(1 - B)$
T	Diffusion temperature	β_γ	Emitter junction injection efficiency $\gamma/(1 - \gamma)$
BV_{CBO}	Collector junction avalanche breakdown voltage	β_T	Total current gain $\beta_B\beta_\gamma/(\beta_B + \beta_\gamma)$
V_d	Junction equilibrium diffusion voltage	γ	Emitter junction injection ratio
		τ	Minority carrier lifetime

Introduction

Modern narrow-base transistors introduce many design and fabrication difficulties not previously encountered in wide-base devices. In particular, the diffusion process for fabricating narrow-base junction transistors cannot be considered invariant; a small perturbation in the location of either an emitter or collector junction will significantly alter the electrical characteristics of such a device. The initial design of a transistor must therefore be directed toward satisfying a given set of parameter specifications, assuming that the associated diffusion process is subject to experimental variations in time, temperature, etc. The purpose of this paper is to present a statistical approach to the solution of this problem, and to demonstrate its applicability to the design of practical semiconductor devices.

In an earlier publication by Kennedy,¹ it was shown that small experimental changes in a diffusion process, from one diffusion run to the next, can significantly contribute to the variability encountered in the physical base width of a transistor. It was also shown that base width variability is, at least in part, a transistor design problem, because this characteristic is closely related to the collector junction location. The present investigation is directed toward a more extensive mathematical study of the foregoing problem. From a one-dimensional analytical model, Monte Carlo methods are used to calculate the variability associated with many transistor parameters. A computer program has been developed to assist in the design and optimization of junction transistors. From a set of parameter specifications for a proposed transistor, and from information pertaining to the experimental tolerances associated with the diffusion process, this computer program calculates the necessary engineering compromise (or trade-off) between eleven transistor parameters, where each parameter exhibits a different degree of sensitivity to process changes.

Results of this analytical investigation establish some of the inherent complexities associated with designing a diffused junction transistor. Transistor variability resulting from a nonideal diffusion process, *where experimental variations exist from one diffusion run to the next*, implies the need of designing a margin-of-safety into each parameter that must satisfy a prescribed specification. Further, results of this investigation show that a satisfactory trade-off between the numerous parameters of a transistor is obtained only through a detailed knowledge of the parameter variability introduced by a proposed diffusion process.

The IBM 7090 computer program developed for this investigation calculates the one-dimensional impurity atom distribution resulting from a prescribed set of basic diffusion parameters. Using this calculated impurity atom distribution, the computer also calculates all the associated transistor parameters outlined in Table 1.

Table 1 Calculated transistor parameters.

Physical base width
Electrical base width*
Emitter junction capacitance**
Collector junction capacitance*
Collector punch-through voltage
Emitter punch-through voltage
Emitter injection efficiency*
Base region transport efficiency*
Current gain*
Collector junction avalanche breakdown voltage
Open-base breakdown voltage

* At an arbitrary collector junction biasing voltage

** Equilibrium

Table 2 Diffusion parameters subject to experimental variations.

C_b	= Bulk impurity atom density in the semiconductor material
C_{01}	= Impurity atom surface concentration for the collector junction diffusion
C_{02}	= Impurity atom surface concentration for the emitter junction diffusion
T_1	= Temperature of collector junction diffusion
T_2	= Temperature of emitter junction diffusion
t_1	= Diffusion time for collector junction
t_2	= Diffusion time for emitter junction

To approximate a non-ideal diffusion process, a proposed set of design-center values is assumed for the diffusion parameters outlined in Table 2. The experimental variations in these diffusion parameters are approximated by a number generator that simultaneously and independently modifies each parameter throughout its specified tolerance limits. Each set of parameters generated in this manner is assumed to characterize a new transistor—or group of transistors—resulting from a given degree of tolerance control in the diffusion process. These sets of diffusion parameters are then used to calculate modified impurity atom distributions, and their associated transistor characteristics (listed in Table 1). This calculation is repeated for several hundred different sets of diffusion parameters, representing the experimental variations experienced in device fabrication, to obtain a statistical picture of the inherent variability associated with a proposed transistor.

The foregoing analytical technique provides a quantitative evaluation of transistor variability as well as a means of designing transistors to a prescribed set of parameter specifications. Upper and lower bounds, representing the imposed transistor specifications, can be placed upon any combination of the calculated transistor parameters listed in Table 1. The computer is programmed so that during a

series of calculations it will count the transistors in a statistical sample which satisfy all imposed parameter specifications. In the design of a transistor, the diffusion parameters listed in Table 2 are systematically modified until a satisfactory combination is obtained—no transistor within the statistical sample is outside the imposed specifications because of experimental variations in its diffusion process. Transistors designed in the foregoing manner automatically contain the necessary margins of safety to assure that they satisfy their parameter specifications when fabricated by the given non-ideal diffusion process.

Analysis

The basic technique used in this analytical investigation is to repeat the same series of transistor parameter calculations (Table 1) upon each impurity atom distribution established by the number generator. Having repeated these calculations for a prescribed sample size, the computer is programmed to automatically calculate a statistical distribution for each individual transistor parameter. Computation speed is clearly an important consideration in a repetitive process of this type. The total time to evaluate a proposed transistor design is proportional to the product of the sample size and the computation time for a single set of transistor parameters.

Although little computer time is required to calculate all of the parameters outlined in Table 1 (approximately 0.45 sec), an unreasonably large amount of material is calculated in this period to adequately describe in a single publication. For this reason, only a brief description will be presented on the mathematical methods used in this analysis; additional details can be obtained from publications listed in the references. The present discussion is intended to present the approximations we have found necessary to attain the required computation speed.

In this analysis the diffusion of donor and acceptor atoms is assumed to be fully characterized by elementary theory in the treatments of Jost, Crank, and Barrer.² A transistor is constructed from semiconductor material of constant impurity atom concentration, C_b , by subjecting the material to two independent diffusion cycles. The first diffusion cycle forms the collector junction by introducing a sufficient number of impurity atoms from a constant source to overcompensate bulk impurities within the semiconductor. A second diffusion forms an emitter junction by overcompensating impurity atoms resulting from the first diffusion; the emitter junction diffusion is assumed to be accomplished by experimental techniques that leave the two diffusions independent of each other. From these assumptions, the total impurity atom distribution within a double-diffused transistor, is described by

$$C(x) = C_b - C_{01} \operatorname{Erfc} [x/2\sqrt{D_1 t_1}] + C_{02} \operatorname{Erfc} [x/2\sqrt{D_2 t_2}], \quad (1)$$

where the diffusion constants D_1 and D_2 are given by expressions of the form

$$D_i = D_{0i} \exp [-\Delta H_i/RT_i]. \quad (2)$$

In any practical diffusion process the so-called constants within Eq. (1) are, in fact, subject to variation from one diffusion run to the next. Table 2 lists the particular parameters assumed to be subject to variation. In the fabrication of transistors an attempt is made to maintain each diffusion parameter at some prescribed design-center value, although tolerance limits must be introduced to characterize adequately a particular laboratory process. This situation has been mathematically approximated by assuming that any individual parameter listed in Table 2 can be statistically described by a normal distribution when viewed over a large number of independent diffusion runs. Each distribution is assumed to be centered upon a specified design-center value, thereby implying a higher probability of occurrence for the desired value than is expressed for the tolerance limits.

As mentioned earlier, the computer program used in this investigation has been designed to accept design-center values of all of the diffusion parameters listed in Table 2, and, in addition, the individual tolerance limits for each parameter. Using this input information, the number generator modifies these design-center diffusion parameters. In this operation the generator is statistically adjusted so that any particular parameter exhibits a normal distribution, over a large number of sets, about its design-center value. The number generator is also adjusted so that 90% of all parameter values lie within their specified tolerance limits, and all values outside these limits are rejected because they represent a situation that is not physically realizable. Figure 1 illustrates the type of impurity atom distribution obtained from a single set of diffusion parameters generated within the computer. The physical base width ($W_p = x_{je} - x_{je}$) is initially established by calculating the two roots of Eq. (1). The actual root locations (x_{je} ; x_{je}) represent the collector and emitter junction transition points; these quantities are used extensively in the calculations to follow.

The space-charge layer characteristics of both the emitter and collector junctions are obtained by solving Poisson's equation throughout the appropriate regions³ of Fig. 1,

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\kappa \epsilon_0}. \quad (3)$$

In this expression the charge distribution $\rho(x)$ is given by

$$\rho(x) = q[C(x) + p(x) - n(x)], \quad (4)$$

where $C(x)$ represents the distribution of ionized impurity atoms, $n(x)$ represents the mobile electron distribution, and $p(x)$ represents the mobile hole distribution. To

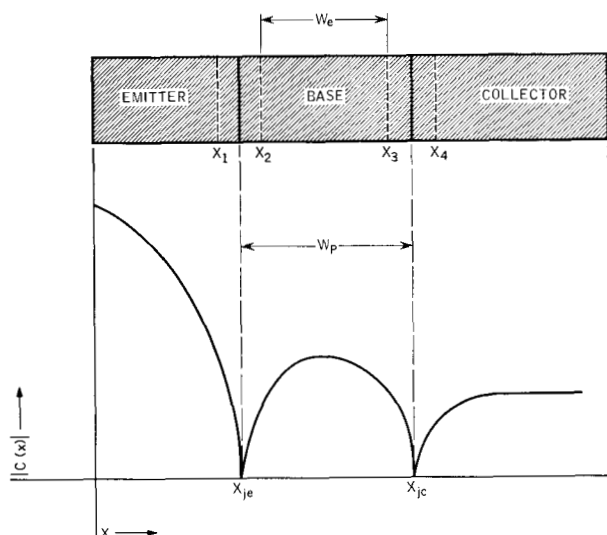


Figure 1 Analytical model of double-diffused transistor.

simplify this calculation, the emitter and collector space-charge layers are assumed to be depleted of mobile charge carriers (holes and electrons), and, furthermore, it is assumed that all the impurity atoms are ionized. From Eq. (3), the resulting space-charge layer electric field distribution can be readily calculated,

$$E(x) = \frac{q}{\kappa \epsilon_0} \int_0^x C(x) dx. \quad (5)$$

A relative location is determined from Eq. (5) for each space-charge layer edge associated with either the collector or emitter junction. For example, if a location x_3 is assumed for the collector junction boundary (Fig. 1), Eq. (5) is integrated to a location x_4 where

$$\int_{x_3}^{x_4} C(x) dx = 0. \quad (6)$$

In addition, the total junction potential, V_T , established by these boundary locations (x_3, x_4), is obtained by a second integration of Eq. (3),

$$V_T = - \int_{x_3}^{x_4} E(x) dx. \quad (7)$$

An identical computational technique is used to establish the equilibrium diffusion potential V_d for both the emitter and collector junctions. Assuming charge neutrality at the collector junction boundaries (x_3, x_4), the diffusion potential V_d is obtained from Eq. (4), providing the locations x_3 and x_4 are known quantities; this potential is given by

$$V_d = \frac{kT}{q} \ln \left\{ \frac{|C(x_3)C(x_4)|}{n_i^2} \right\}. \quad (8)$$

Because the locations x_3 and x_4 are unknown quantities, Eqs. (6), (7), and (8) are iterated until the total junction potential V_T equals the equilibrium diffusion potential V_d thus satisfying the equality

$$\frac{kT}{q} \ln \left\{ \frac{|C(x_3)C(x_4)|}{n_i^2} \right\} = \left| \int_{x_3}^{x_4} E(x) dx \right|. \quad (9)$$

Boundaries can be readily located from the foregoing equations for both the emitter and collector junctions. From this information junction capacities are established using a parallel-plane approximation, and the electrical base-width (Fig. 1) is established from $W_e = (x_3 - x_2)$. To simplify both the electrical base-width calculations and the junction capacity calculations, the emitter junction is assumed to be at equilibrium while the collector junction is reverse biased to some specified voltage.

Equations (1) through (9) are also used to calculate the punch-through voltage for either the collector or emitter junction.³ In this analysis the collector junction punch-through voltage is defined as the collector voltage at which the collector junction space-charge layer just encounters the equilibrium emitter junction space-charge layer (or when $x_2 = x_3$ in Fig. 1) with the emitter junction at equilibrium. Similarly, the emitter junction punch-through voltage is defined as the reverse biasing potential required at the emitter to force $x_2 = x_3$, when the collector junction is at equilibrium. Both of these calculations are accomplished in essentially the same manner. After locating all space-charge layer edges, for an equilibrium transistor, and also the associated diffusion potentials V_d , the condition $x_2 = x_3$ is introduced with the emitter, and then the collector, at equilibrium. By integrating Eq. (7) across the appropriate non-equilibrium junction, and then subtracting its diffusion potential, the punch-through voltage is readily calculated.

A rigorous calculation of either the emitter injection efficiency or the base region transport efficiency is an exceedingly difficult task, as reported by Kennedy and Murley.^{4,5} The difficulty arises inasmuch as the injection characteristics of a diffused junction are a consequence of its "built-in" drift field which in Fig. 1 is due to conductivity grading within the semiconductor material. Further, this "built-in" drift field can alter the characteristics of minority carrier transport across the base region of a diffused junction transistor. To calculate these transistor parameters, it is therefore necessary to assume that drift and diffusion contribute to the transport of minority carriers within the base and emitter regions of a transistor:

$$J_p(x) = -q D_p \left\{ \frac{dp}{dx} - p(x) \sum_{n=0}^{\infty} A_n (x - x_0)^n \right\} \quad (a) \quad (10)$$

$$J_n(x) = q D_n \left\{ \frac{dn}{dx} + n(x) \sum_{n=0}^{\infty} B_n (x - x_0)^n \right\}. \quad (b)$$

In Eq. (10) the "built-in" drift field is represented by a Taylor series. Upon substituting Eq. (10) into the expressions for hole and electron continuity,

$$\frac{dJ_p}{dx} + \frac{qp(x)}{\tau_p} = 0 \quad (a) \quad (11)$$

$$\frac{dJ_n}{dx} - \frac{qn(x)}{\tau_n} = 0, \quad (b)$$

a pair of differential equations is obtained, one for the emitter region and one for the base region; these equations can be solved by series techniques. Using this method, equations are obtained for the base and emitter region minority carrier distributions that satisfy appropriate boundary conditions at the emitter and collector depletion layer edges and also at the emitter region ohmic contact. From these minority carrier distribution equations, both the emitter injection efficiency, β_γ , and the base region transport efficiency, β_B , can be established for a given transistor.

The above method requires a long computation time to establish either the emitter injection efficiency or the base region transport efficiency. To alleviate this difficulty approximation equations are used. Even though the approximation equations provide a substantial decrease in time, the accuracy is inadequate for most practical requirements. The similarity between all transistors associated with a single set of design-center diffusion parameters provides a means of improving this accuracy without significantly increasing the total computation time. Using Eqs. (10) and (11) upon a maximum of three devices for each set of design-center diffusion parameters, one establishes and applies correction factors to each approximate calculation.

The emitter injection efficiency is calculated using the approximation formula⁶

$$\beta_\gamma = \frac{D_p I_n^2 [C'(x_1)]}{D_n \bar{N}} \left\{ 1 + \frac{\ln [(x_{je} - x_1)/x_{je}]}{\ln [C(0)/C(x_1)]} \right\} \quad (12)$$

where

$$\beta_\gamma = \frac{\gamma}{1 - \gamma}; \quad \bar{N} = \left| \int_{x_2}^{x_3} C(x) dx \right|. \quad (13)$$

The correction factors applied to Eq. (12) result from observations of the calculated variability attributed to β_γ . It has been observed that most variations in the emitter injection efficiency, due to the diffusion process, are attributable to variations in the electrical base width. It is also observed that these variations in the electrical base width result from changes in the collector junction location, which implies that the error introduced by Eq. (12) will be a constant for all devices associated with a given set of design-center diffusion parameters. Recognizing this characteristic, one establishes a correction factor by a single application of Eqs. (10) and (11) to the design-center

diffusion parameters; this factor is used to correct all values of β_γ calculated by Eq. (12).

Similar approximation methods have been used to calculate the base-region transport efficiency. Each transistor associated with a given set of design-center diffusion parameters is assumed to have no base-region drift field, and thus its base-region minority carrier transport efficiency is given by

$$\beta_B = 2(L_p/W_e)^2. \quad (14)$$

After this calculation, three transistors are selected from the statistical sample: the device exhibiting the widest base width, the device exhibiting the narrowest base width, and also a device representing the design-center transistor. For these three structures, a more detailed calculation of β_B is conducted, using Eqs. (10) and (11). The three rigorous calculations of base-region transport provide a correction factor that can be used, by a linear interpolation, to correct all the values of β_B established by the approximate formula Eq. (14). A maximum error of 5% of β_B is encountered with this method, and the computation time is substantially decreased.

The basic technique used to calculate the collector junction avalanche breakdown voltage has been previously described by Kennedy and O'Brien⁷. The collector junction space-charge layer electric field distribution is established from Eq. (5), and thus carrier multiplication, M , is obtained from the integral

$$1 - \frac{1}{M} = a \int_{x_3}^{x_4} \exp [-b/E(x)] dx, \quad (15)$$

where a and b are empirical constants that have been established for both germanium and silicon. In this calculation the collector junction space-charge layer edge, x_3 , is iterated until Eq. (15), when used in conjunction with Eq. (5), becomes unity, and thus $M = \infty$. From these

Table 3 Assumed parameters for a typical non-ideal transistor fabrication process.

Bulk material (n-type)	$C_b = 1.5 \times 10^{16} \pm 0.375 \times 10^{16}$
Boron	$C_{01} = 4.5 \times 10^{18} \pm 1.25 \times 10^{18}$
	$T_1 = 1300^\circ\text{C} \pm 2^\circ\text{C}$
	$D_{01} = 15.8$
	$\Delta H_1 = 88.8$
Phosphorus	$C_{02} = 4.5 \times 10^{20} \pm 1.25 \times 10^{20}$
	$T_2 = 1100^\circ\text{C} \pm 2^\circ\text{C}$
	$D_{02} = 10.5$
	$\Delta H_2 = 85.0$
Minority carrier diffusion length	$L_p = 4 \times 10^{-4} \text{ cm}$
	C in atoms/cm ³
	D in cm ² /sec
	ΔH in kilo-cal

space-charge layer edge locations Eq. (7) is used to determine the applied junction voltage at which carrier multiplication becomes infinite; this situation approximates the collector junction avalanche breakdown voltage.

Numerical integration techniques are too slow when applied to Eq. (15). To solve this problem we have therefore used approximation methods which provide adequate computational accuracy. The approximation method used here is the three-point Gaussian quadrature,⁸ reducing Eq. (15) to the following form:

$$a \int_{x_3}^{x_4} \exp [-b/E(x)] dx \\ = a \left\{ \frac{8}{9} \exp [-b/E(x_m)] + \frac{5}{9} \exp [-b/E(x_m - x_a)] \right. \\ \left. + \frac{5}{9} \exp [-b/E(x_m + x_a)] \right\} (x_m - x_3)/2, \quad (16)$$

where

$$x_a = (0.774597)(x_m - x_3)/2. \quad (17)$$

The term x_m represents the point of maximum space-charge layer electric field within the collector junction. In many situations Eq. (16) is sufficiently accurate for an avalanche breakdown calculation (approx. 1%). Transistors exhibiting an exceedingly unsymmetrical collector junction space-charge layer often require an additional three-point calculation on the collector region side of the structure.

The last parameter calculated for each transistor is the open-base breakdown voltage. This parameter is given by the collector junction space-charge layer edge locations (x_3 ; x_4) that satisfy the equality⁹

$$1 = a'[\beta_T(W_e) + 1] \int_{x_3}^{x_4} \exp [-b'/|E(x)|] dx, \quad (18)$$

where a' and b' are experimentally determined constants characterizing low level multiplication in the collector junction. The similarity between Eqs. (15) and (18) permits the use of essentially identical computational techniques for avalanche breakdown and open-base breakdown; the difference between these parameter calculations resides in the current gain parameter $\beta_T(W_e)$ in Eq. (18). For this situation it is again necessary to use an approximation formula, Eqs. (12) and (14), and to introduce corrections for changes in electrical base width, through a linear interpolation. Although this particular interpolation is relatively inaccurate (about 10% error in the total current gain β_T) open-base breakdown is a slow function of current gain, and therefore a negligible error is introduced in the calculated breakdown voltage.

Variability of transistor parameters

The parameter variability of a diffused junction transistor cannot be characterized by an elementary mathe-

matical equation or by any single graphical illustration. The conclusions of this investigation are therefore presented through illustrative calculations upon diffused junction transistors resulting from a typical non-ideal diffusion process (Table 3). To demonstrate some of the design factors that influence transistor variability, the collector and emitter junction locations within these illustrative structures are systematically changed throughout a range that approximates many practical semiconductor devices.

A small degree of correlation exists among the parameter variations encountered in any diffusion process. This correlation is usually a consequence of temperature variations. Such correlation has been neglected in this analysis because it represents a negligible source of parameter variability, in the presence of practical experimental tolerances. Furthermore, it should also be noted that temperature variation (which is the principal source of correlation) is a very small fraction of the diffusion temperature (0.2% or less). Of all the diffusion parameters used in this analysis, the fractional variation of the diffusion temperature is smallest, by at least an order of magnitude.

In the following examples, it is assumed that boron is first diffused into *n*-type silicon thereby forming the collector junction. The boron diffusion is followed by a phosphorus diffusion to form an emitter junction. Published values are used for the activation and diffusion constants of both phosphorus¹⁰ and boron.¹¹

The first example in this series of calculations demonstrates some of the inherent difficulties associated with the design and fabrication of narrow base transistors. The example illustrates further that a deeply diffused narrow base transistor will often represent a completely impractical semiconductor device. Using the diffusion parameters outlined in Table 3 a collector junction is fixed at 200 μ -inches from the semiconductor surface. In these calculations the emitter is first located 50 μ -inches from the surface and is then stepped in 10- μ -inch intervals to a depth of 160 μ -inches. At each emitter junction location the magnitude and the variability are calculated for all transistor parameters listed in Table 1.

A second illustrative example demonstrates the inherent advantages in designing narrow base transistors so that their emitter and collector junctions are relatively close to the semiconductor surface. Using the diffusion parameters outlined in Table 3 the resulting transistor is adjusted to have a design-center physical base width of 60 μ -inches, while the collector junction depth is stepped in 10- μ -inch intervals between 80 and 200 μ -inches. At each collector junction location both the magnitude and the variability are calculated for all transistor parameters listed in Table 1.

Basic difficulties arise in presenting the results of these calculations because no single statistical measurement is

capable of fully characterizing the variability of all transistor parameters. Many parameters, for example, are not symmetrically distributed about their design-center values. In some situations the design-center value of a transistor parameter cannot even be established because of masking by another parameter—for example, when collector junction avalanche breakdown is masked by collector junction punch-through. In the following discussions the variability of a transistor parameter is established, when possible, in terms of a variability index that characterizes the parameter distribution relative to its design-center value. For each transistor parameter a design-center value, P , is calculated and, in addition, a range, ΔP , is also calculated which contains the central 90% of all values within a given statistical sample. The variability index has been defined as $\Delta P/P$, and it is expressed in percentage. In special situations it becomes necessary to introduce additional qualifying information to describe adequately this parameter variability. Situations of this kind are discussed individually.

Figure 2 presents the calculated characteristics of a transistor that is only suitable as a wide base device. In this example the collector junction design-center has been held at a depth of 200 μ inches, making the collector junction location extremely sensitive to experimental variations in the diffusion process.¹ In deep structures of this type the equilibrium electrical base width, W_e , (Fig. 2) can become a very small part of the physical base width (when W_p is 40 μ inches W_e is 5.4 μ inches); this situation implies the presence of an intolerable variability in all transistor parameters. In Fig. (2b) a decreased physical base width results in an increase of the physical base width variability ($\Delta W_p/W_p$) but, at the same time, a substantially greater increase is observed in the variability associated with all other transistor parameters. If a 60- μ inch physical base width is used in this particular transistor, the design-center collector punch-through voltage becomes 53 volts with 237% (125 volts) variability. Transistors designed in this manner would exhibit an intolerable spread in their punch-through voltage because 90% of all units lie between 5.0 and 132 volts.

Table 4 presents a more detailed view of the narrow base (60- μ inch) transistor that has a deep collector junction (200 μ inches). To permit a comprehensive evaluation of such a device, Table 4 lists design-center values for each of its parameters together with their respective variability range. Table 4 shows that this transistor has a design-center collector punch-through voltage of 53 volts and an open-base breakdown voltage of 45 volts—one of these parameters usually establishes its maximum operating voltage. Further, the design-center current gain of 64 certainly represents a value that is satisfactory for many practical applications. If, instead, this transistor is viewed in terms of its parameter variability, a completely differ-

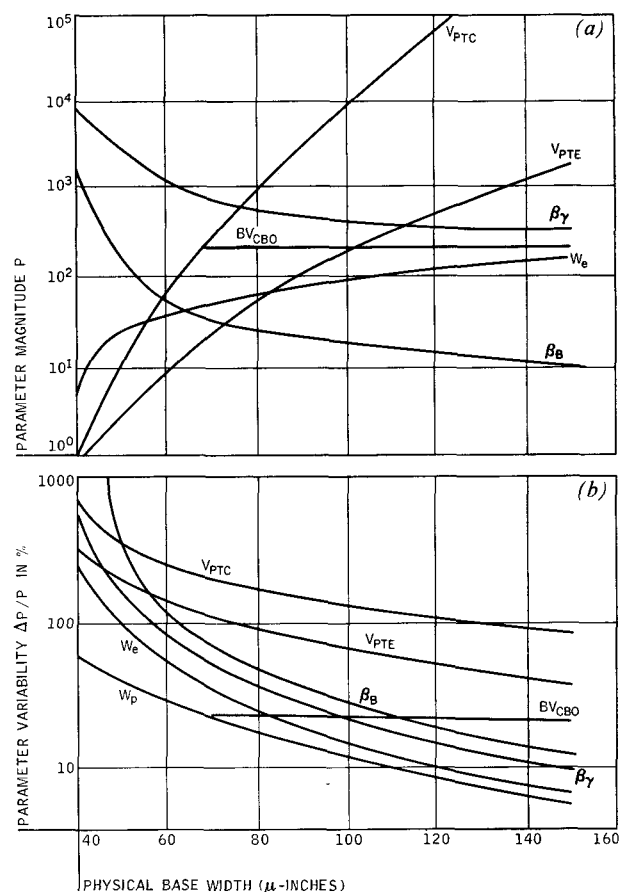


Figure 2 (a) Calculated design-center transistor parameters (P) with $x_{jc} = 200$ μ inches. The diffusion parameters for this calculation are outlined in Table 3. The parameters V_{PTC} , V_{PTE} are in volts, W_e is in μ inches and β_γ , β_B are dimensionless. (b) Transistor parameter variability ($\Delta P/P$) from a statistical sample of 500 devices. ΔP represents the parameter range containing 90% of the values.

ent opinion will be obtained regarding its potentialities. This point is, however, highly subjective and is dependent upon the amount of fabrication loss considered to be tolerable. Since transistors can usually be designed to exhibit a negligible theoretical fabrication loss, the point of view has been taken that no circuit parameter specification of a transistor should reside within its calculated variability range. From Table 4 it therefore is assumed that the above transistor design should not be expected to satisfy an operating voltage specification in excess of 5 or 10 volts, depending upon either punch-through or open-base breakdown, or a current gain specification in excess of 7.5.

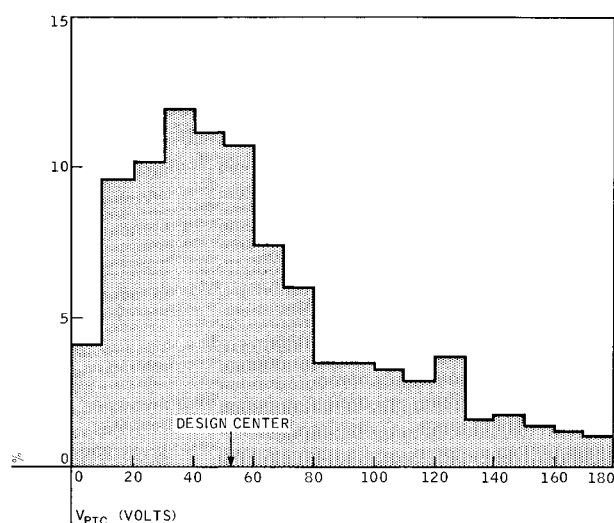


Figure 3 Distribution of the collector punch-through voltage (V_{PTC}) when $W_p = 60$ μ inches and $x_{je} = 200$ μ inches. This calculation is based upon a statistical sample of 1000 transistors using the diffusion parameters outlined in Table 3.

Figure 3 illustrates the resulting distribution of collector punch-through voltage upon a statistical sample of 1000 units that have the foregoing design-center physical base width of 60 μ inches. The variability range of this particular parameter is unsymmetrically distributed about its design-center value. Of this sample, 57% (570 transistors) are distributed within the range 0 to 53 volts; 43% (430 transistors) lie between 53 and 225 volts. It should be noted that during this calculation no device was found to exhibit collector punch-through at transistor equilibrium. The above situation has been observed in any transistor parameter having a variability in excess of 200%; an unsymmetrical distribution usually limits the number of transistors exhibiting a parameter magnitude of zero.

Table 5 illustrates the sensitivity of the 60- μ inch base-width transistor to the individual diffusion parameters listed in Table 3. When the specified tolerance limits are introduced for one diffusion parameter at a time, while all others are held constant, the specific diffusion parameters can be observed that represent the principal contributors to a given transistor variability characteristic. For this particular transistor, decreasing the tolerance limits upon C_{01} would represent a good "first-step" to decrease fabrication variability, while decreasing these limits upon C_b would exhibit a negligible effect. When this method of process evaluation is used, such calculations (Table 5) are directly applicable to process improvement programs directed toward decreasing variability and increasing fabrication yield for a given transistor.

Table 4 Transistor characteristics resulting from a non-ideal diffusion process (Table 3).

$$x_{je} = 200 \mu\text{inches}$$

Parameter	Design-center value	Range for 90% of devices
Physical base width	60	50-70
Electrical base width	34	22-45
Emitter junction capacitance	0.180	0.145-0.21
Collector junction capacitance	0.061	0.057-0.065
Collector punch-through voltage	53	5.0-132
Emitter punch-through voltage	9.5	2.0-15
Emitter injection efficiency	1160	790-1870
Base region transport efficiency	68	7.5-100
Current gain	64	7.5-100
Open-base breakdown voltage	45	10-69

Cap. in pF/mil²
 Voltages in volts
 Length in μ inches

Table 5 Transistor variability characteristics.

$$W_p = 60 \mu\text{inches} \quad x_{je} = 200 \mu\text{inches}$$

Transistor Parameter	Diffusion variable, in percent					
	C_{01}	C_{02}	C_b	T_1	T_2	ALL
W_p	19	10	9.3	14	14	31
W_e	40	20	12	33	28	67
V_{PTC}	174	69	39	107	108	237
V_{PTE}	105	50	14	77	76	157
C_e	*	*	11	*	*	11
C_b	20	87	18	17	10	38
β_B	62	36	18	56	44	136
β_γ	45	29	7.5	38	31	93
β_T	60	36	17	54	43	121
BV_{CEO}	75	43	33	67	50	130

* Less than 1

In previous discussions no mention was made of the open-base breakdown voltage and its variability with changes in physical base width. Unlike many parameters, open-base breakdown is both directly and indirectly related to other transistor parameters in both magnitude and variability. Consider for example a wide-base transistor that exhibits a calculated punch-through voltage of many thousands of volts (Fig. 4). In this type of tran-

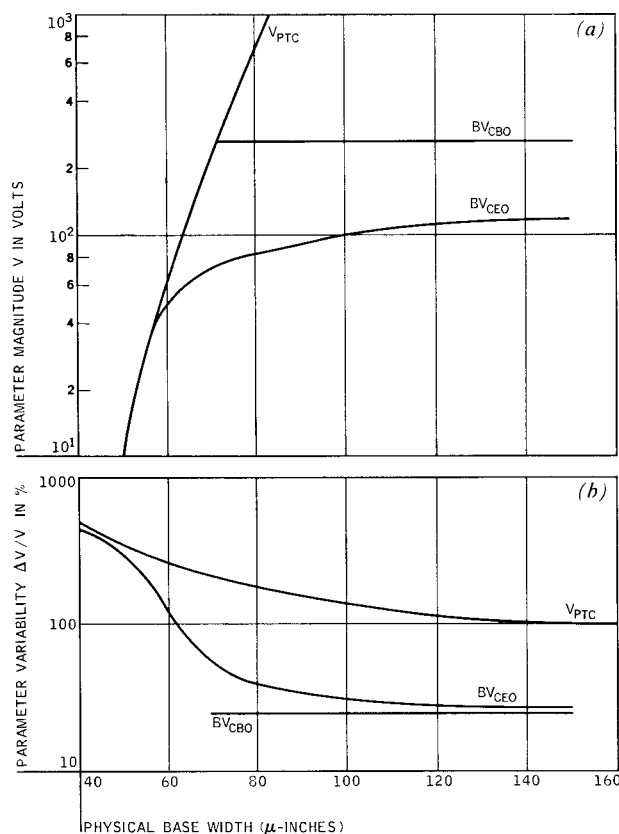


Figure 4 (a) Calculated design-center values for the transistor open-base breakdown voltage (BV_{CEO}), collector junction punch-through voltage (V_{PTC}) and the collector junction avalanche breakdown voltage (BV_{CBO}). This calculation is based upon the diffusion parameters outlined in Table 3 with $x_{je} = 200$ μinches. (b) Calculated parameter variability ($\Delta V/V$) from a statistical sample of 500 units. ΔV represents the parameter range containing 90% of all values.

sistor, open-base breakdown is closely related to the collector junction avalanche breakdown voltage in magnitude (Fig. 4a) and in variability (Fig. 4b); it is also a weak function of current gain. At a base width of 140 μinches the variability of open-base and avalanche breakdown (Fig. 4b) differ only by the dependence of open-base breakdown upon current gain. A decreased physical base width substantially alters this situation. The interrelations among the parameters open-base breakdown, current gain, collector punch-through, and collector junction avalanche breakdown, result in a reduction of the open-base breakdown voltage (Fig. 4a) until it is nearly equal to the collector punch-through voltage. Further, the reduced physical base width results in an open-base break-

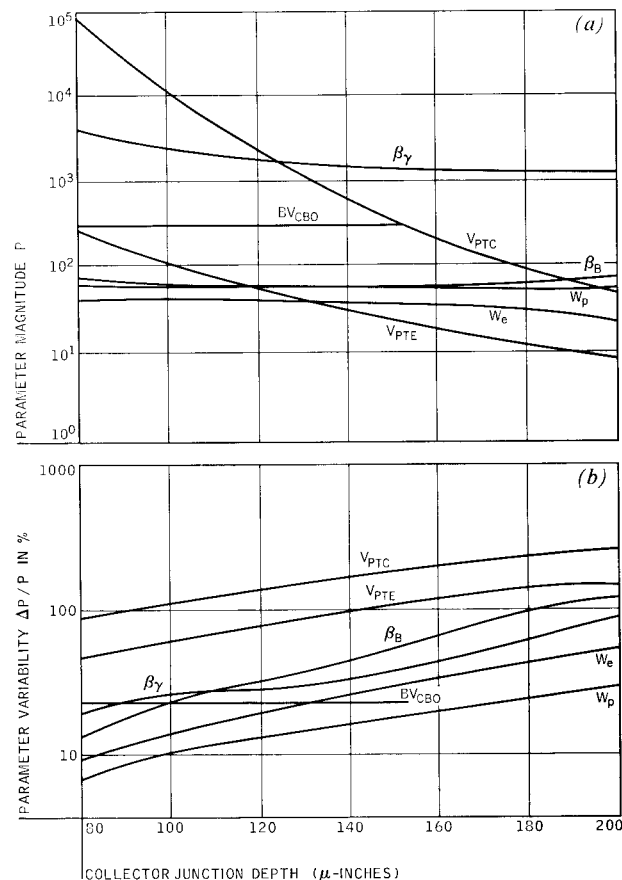


Figure 5 (a) Calculated design-center transistor parameters (P) with $W_p = 60$ μinches. The diffusion parameters for this calculation are outlined in Table 3. The parameters V_{PTC} , V_{PTE} are in volts; W_e is in μinches, and β_γ , β_B are dimensionless. (b) Transistor parameter variability ($\Delta P/P$) from a statistical sample of 500 devices. ΔP represents the parameter range containing 90% of all values.

down voltage variability that is governed by the collector punch-through voltage (Fig. 4b). It is for this reason that transistors required to satisfy a minimum open-base breakdown voltage specification must be designed to have what initially appears to be an unreasonably large punch-through voltage. The inherently large variability in the collector punch-through voltage should not force transistors outside their open-base breakdown specification.

A few of the difficulties associated with deep emitter and collector junctions have been discussed. Next in line of discussion are some of the design directions leading to a more satisfactory narrow-base transistor. In this example an illustrative semiconductor structure has been used of the type previously outlined in Tables 3 and 4. Parameter

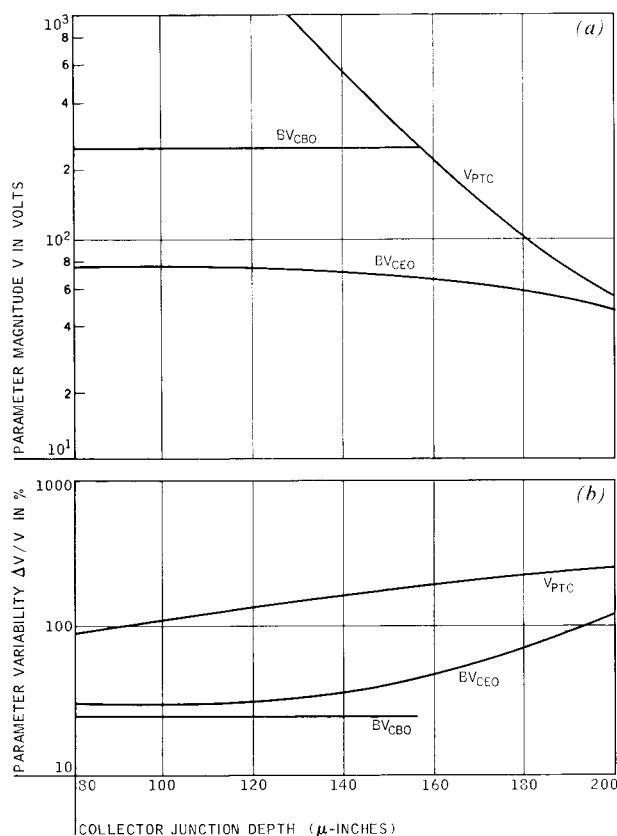


Figure 6 (a) Calculated design-center values for the transistor open-base breakdown voltage (BV_{CEO}), collector junction punch-through voltage (V_{PTC}) and the collector junction avalanche breakdown voltage (BV_{CBO}). This calculation is based upon the diffusion parameters outlined in Table 3 with $W_p = 60$ μ -inches. (b) Calculated parameter variability ($\Delta V/V$) from a statistical sample of 500 units. ΔV represents the parameter range containing 90% of all values.

magnitude and variability calculations have been made for collector junction depths of 80 to 200 μ -inches while, at the same time, the physical base width is held at 60 μ -inches. Although these calculations are based upon a constant physical base width, a decreased collector junction depth is shown to increase the electrical base width as in Fig. 5a; this indicates that an increase should also be observed in both the emitter and collector punch-through voltages.

Many of the difficulties previously ascribed to a deeply diffused narrow base transistor are readily eliminated by reducing the collector junction diffusion depth. Figure 5a shows that the most troublesome parameters in a deeply diffused structure, e.g., collector junction punch-through voltage, are no longer a serious problem. In the

present example, decreasing the collector junction depth from 200 to 100 μ -inches increases the punch-through voltage from 53 volts to 11,100 volts. Figure 5b illustrates that a general reduction is obtained in the variability of all transistor parameters, thereby implying an overall improvement in the useful operating characteristics of such a device.

The maximum operating voltage of any given transistor is often determined by its open-base breakdown voltage. This parameter, therefore, is of particular interest. A reduction in the collector junction diffusion depth significantly increases the open-base breakdown voltage (Fig. 6a) and, furthermore, a design modification of this kind also reduces the inherent variability attributed to this transistor parameter (Fig. 6b). Because of the complicated relation between collector junction punch-through and open-base breakdown, a decrease in the collector junction depth from 200 μ -inches to 100 μ -inches increases the open-base breakdown voltage from 45 to 73 volts and decreases its variability from 130% to 29%.

To provide a direct comparison of the improvements obtained by a 100- μ -inch collector junction location, Table 6 lists the resulting design-center transistor parameters together with their respective variability ranges. A substantial improvement is obtained by applying to this transistor the same basis of evaluation previously applied to the deep structure (Table 4). The 100- μ -inch collector junction depth yields a transistor exhibiting a minimum operating voltage of 63 volts, based upon its open-base breakdown voltage, and a minimum current gain of 55. It should be observed that the present transistor (Table 6)

Table 6 Transistor characteristics resulting from a non-ideal diffusion process (Table 3).

$$x_{je} = 100 \mu\text{inches}$$

Parameter	Design-center value	Range for 90% of devices
Physical base width	60	56-63
Electrical base width	45	41-58
Emitter junction capacitance	0.62	0.56-0.68
Collector junction capacitance	0.072	0.067-0.076
Collector junction avalanche breakdown	267	227-306
Collector punch-through voltage	11,100	5000-17,000
Emitter punch-through voltage	105	72-138
Emitter injection efficiency	2,110	1,870-2,360
Base region transport efficiency	63	56-71
Current gain	61	55-68
Open-base breakdown voltage	73	63-94
Cap. in pF/mil ²		
Voltages in volts		
Length in μ -inches		

Table 7 Transistor variability characteristics.

$$W_p = 60 \mu\text{inches} \quad x_{jc} = 100 \mu\text{inches}$$

Diffusion variable in percent						
	C_{01}	C_{02}	C_b	T_1	T_2	ALL
W_p	8.4	3.6	4.8	3.8	5.5	13
W_e	13	5.2	4.5	5.7	7.4	18
V_{PTC}	113	32	34	42	40	126
V_{PTE}	60	19	1.7	21	23	70
BV_{CBO}	*	*	23	*	*	25
C_c	*	*	12	*	*	12
C_e	16	3.8	*	6.4	4.4	20
βV	17	8.3	5.1	8.0	12	26
β_{γ}	19	11.2	*	4.8	9.8	27
β_T	17	8.4	5	8	12	26
BV_{CEO}	4.3	*	26	*	1.2	29

* Less than 1

exhibits this increased useful current gain, in comparison with the device outlined in Table 4, despite a slight reduction in its design-center value. Further, Table 7 provides the parameter variability of this particular device resulting from the variation of one diffusion parameter at a time. This calculation shows that C_{01} , as before, represents a principal source of fabrication difficulty.

Transistor design

Previous discussions of parameter variability have established some of the inherent difficulties encountered in designing a diffused junction transistor. Although the design-center parameters of a proposed device may adequately satisfy its parameter specifications, this fact alone is insufficient to assure a reasonable fabrication yield. It is therefore suggested that neglecting parameter variability in the initial design of many transistors does not avoid the problem but, instead, it frequently implies the necessity of redesigning during production. To attain a satisfactory fabrication yield it is often necessary to modify systematically the initial design of a transistor. The systematic modification is guided by parameter distributions resulting from measurements upon a large number of devices instead of an idealized set of design-center characteristics.

The following technique for designing diffused junction transistors is similar, in principle, to designing upon a large-scale production line, except that transistor fabrication is simulated by a digital computer. Using previously described methods to approximate a non-ideal diffusion process, one programs the computer to determine the total number of devices in a given statistical sample that satisfy an imposed set of parameter specifications. Device design is accomplished by systematically modifying the

design-center values of two diffusion parameters at a time, thereby establishing a two-dimensional matrix that exhibits regions of high and low yield to the given parameter specifications. On the assumption of no prior knowledge of the proper values for these diffusion parameters, a matrix is first formed throughout a wide range of values, with relatively large intervals for each parameter. After the establishment of a general range of diffusion parameter values that will yield the required transistors, a second matrix is calculated throughout this range. This second transistor design matrix has small diffusion parameter intervals, thus providing the necessary details to permit an optimization of the structure.

The large number of variables associated with any diffusion process indicates that the above calculation could, in theory, become a formidable task. In practice, however, very few of these variables are actually independent, thereby simplifying this computational problem. Standard laboratory practices frequently dictate one or both of the impurity atom surface concentrations (C_{01} or C_{02}) and, furthermore, practical requirements expected upon the resulting transistor often place restrictions upon its geometrical properties, e.g., the physical base width. In many situations transistor design is a relatively easy computational task because the problem is reduced to a study of two or three independent diffusion parameters.

An important part of any transistor design problem is the determination of satisfactory "effective" minority carrier diffusion lengths for use during the current gain calculations. As described in the earlier literature,⁵ an identical minority carrier diffusion length can be assumed within the base and emitter region of a transistor; this approximation is used extensively. Further, the base region minority carrier diffusion length is adjusted to provide agreement between the theoretical and experimentally determined current gain of transistors fabricated by the particular diffusion system under consideration. In these experiments current gain is measured as a function of collector current. A value is selected above the low current region of the transistor yet below its high current region where base-region conductivity modulation is evident. This method is clearly an approximation, although it offers little difficulty if the device to be designed is a small variation upon these experimental units. In this instance the theoretically predicted current gain will be in substantial agreement with the experimentally determined value. If, however, the required transistor represents a large variation upon such experimental units, the design calculations are then conducted in two steps. A tentative design is established using an initially determined minority carrier diffusion length. After completion of the first laboratory models based upon the tentative design, a new minority carrier diffusion length is established by comparing their measured and calculated current gain. Using this

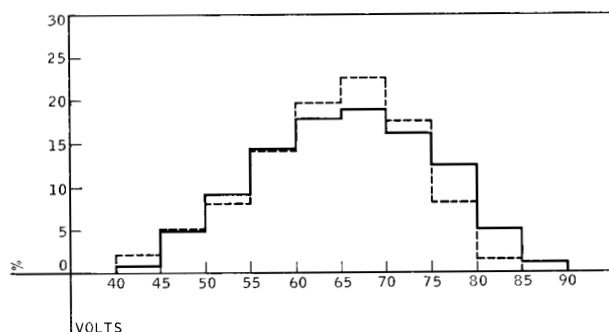


Figure 7 A comparison between the measured and calculated open-base breakdown voltage for a statistical sample of 575 core-driver transistors.

..... experimental
 ————— calculated

revised value of minority carrier diffusion length, a final design is established. Effectively the final device design will be a small variation upon the devices fabricated in accordance with the tentative design.

This method for determining an appropriate "effective" minority carrier diffusion length is based upon the assumption that the theoretically calculated transistor is a good characterization of the devices upon which such current gain measurements are conducted. By comparing the measured and calculated design-center parameters for these transistors, the validity of this assumption is tested. Because of the large sensitivity of a transistor to changes in its diffusion parameters, the initially calculated theoretical characteristics of a particular device can be expected to differ from their measured values. As a next step, appropriate diffusion parameter modifications are determined from variability calculations of the type illustrated in Tables 5 and 7. It should be emphasized that these modifications are usually very small, and the final values lie within the uncertainty limits of laboratory measurements. The "effective" minority carrier diffusion length is established only after satisfactory agreement is obtained between the calculated and measured characteristics of the initializing transistors.

Figures 7 and 8 illustrate the degree of agreement obtained between theory and experiment, after fitting the calculated distribution curves in the above manner. Figure 7 presents the measured and calculated distribution of open-base breakdown for a sample of 575 core-driver transistors. The measured devices represent a random selection of transistors from an existing large scale manufacturing facility, containing many different diffusion runs for this particular device. Similarly, Fig. 8 illustrates the measured current gain for a different sample of 145 units from this same manufacturing facility; the calculated distribution is for a larger statistical sample (575 units)

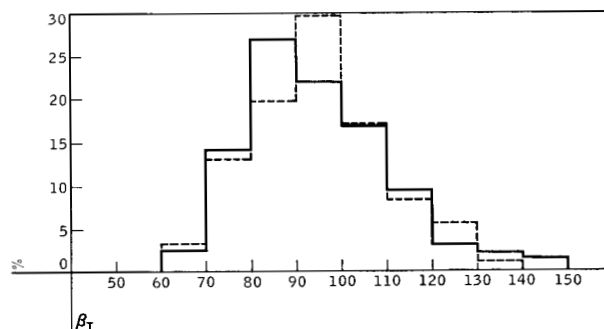


Figure 8 A comparison between the measured and calculated current gain (β_T) for core-driver transistors: experimental sample size 145 units, theoretical sample size 575 units.

..... experimental
 ————— calculated

which is consistent with the sample size used in Fig. 7.

In this comparison between theory and experiment, all design-center diffusion parameters, and their variabilities, were taken from manufacturing specifications for the particular transistor under consideration. This manufacturing specification contains a design-center value, and also the individual tolerance limits for each diffusion parameter. The input data for these computer calculations were taken directly from this set of manufacturing specifications.

Two illustrative examples are used to demonstrate the proposed method of designing diffused junction transistors. The first example applies the diffusion parameters outlined in Table 3, except for a permitted change in C_b , to the design of a high voltage transistor. Using an assumed minority carrier diffusion length of 4×10^{-4} cm, the proposed device must exhibit a current gain in excess of 30 and an open-base breakdown voltage in excess of 125 volts; these parameter specifications must be satisfied with a maximum C_b . A second example consists of designing a very narrow base transistor (20- μ inch) with a minimum current gain specification of 75—assuming a minority carrier diffusion length of 2×10^{-4} cm—and with a minimum open-base breakdown specification of 20 volts.

Table 8 presents the two variable design matrices for this high-voltage transistor. The upper matrix establishes the percentage of units within the statistical sample (500 transistors) that simultaneously satisfy the parameter specifications $\beta_T \geq 30$ and $BV_{CEO} \geq 125$ volts; the matrix here was calculated for a wide range of physical base widths ($25 < W_p < 150$ μ inches) and bulk material resistivities. The principal purpose of this first matrix is to determine a general range for the independent variables that will yield transistors capable of satisfying the imposed parameter specifications. The region of particular interest

Table 8 Two variable design matrix—high voltage transistor.

$$x_{je} = 50 \text{ } \mu\text{inches}, \beta_T \geq 30, BV_{CEO} \geq 125 \text{ Volts}$$

Fabrication yield in percent						
Bulk material resistivity (ohm-cm)	Physical base width (μ inches)					
	25	50	75	100	125	150
4	0	0	0	0	0	0
6	0	3	57	0	0	0
8	0	45	100	0	0	0
10	0	93	100	0	0	0
12	0	100	100	0	0	0
	Physical base width (μ inches)					
	40	50	60	70	80	90
6	0	3	19	45	72	5
7	0	14	60	90	99	11
8	3	45	92	100	100	16
9	8	80	100	100	100	25
10	20	93	100	100	100	31

in this matrix is bounded on two sides by limitations due to the physical base width, and on a third side by a lower limit upon the bulk material resistivity. Devices with a physical base width of 25 μ inches (or less) exhibit a low open-base breakdown voltage due to a low collector punch-through voltage. In contrast, transistors with a physical base width of 100 μ inches (or more) cannot satisfy the current gain specification. The third boundary upon this region, i.e., bulk material of 4 ohm-cm (or less), is due to devices with a low open-base breakdown voltage resulting from an increased carrier multiplication in the collector junction space-charge layer.

The lower matrix in Table 8 presents a detailed calculation of the diffusion parameter ranges from which satisfactory transistors can be obtained. This matrix indicates that transistors with a 70- μ inch base width and a bulk material resistivity of approximately 9 ohm-cm will satisfy the parameter specifications with an adequate margin-of-safety. Table 9 presents the calculated design-center characteristics of this particular transistor, indicating the resulting trade-off of various parameters to satisfy the required specifications. Because a specification was placed upon the minimum open-base breakdown voltage, the design-center collector junction punch-through voltage is very large (16,100 volts). This value prevents the excessive variability of the punch-through voltage from influencing open-base breakdown. In this proposed transistor design, open-base breakdown has the variability of collector

Table 9 Design-center characteristics—high voltage transistor.

Physical base width	70 (μ inches)
Electrical base width	51.3 (μ inches)
Emitter junction capacitance	0.51 (pF/mil ²)
Collector junction capacitance	0.048 (pF/mil ²)
Collector punch-through	16,100 (volts)
Emitter punch-through	85.6 (volts)
Emitter injection efficiency	1,726
Base region transport efficiency	51.2
Current gain	49.7
Collector junction avalanche breakdown	552 (volts)
Open-base breakdown	171 (volts)

junction avalanche breakdown thus permitting a small margin-of-safety over the parameter specification $BV_{CEO} \geq 125$ volts. In addition, the electrical base width has been adjusted so that its variability will not result in transistors with a current gain less than 30.

Table 10 illustrates a second transistor design example which is also based upon the diffusion parameters outlined in Table 3, except for the bulk impurity atom density C_b and the minority carrier diffusion length L_p . In this example design specifications have imposed an exceedingly narrow base width (20 μ inches) and a relatively large open-base breakdown voltage (20 volts). The specifications in this instance have forced the use of a very shallow structure. Consistent with previous calculations, a shallow emitter junction increases the collector punch-

Table 10 Two variable design matrix—narrow base transistor.

$$W_p = 20 \text{ } \mu\text{inches}, \beta_T \geq 75, BV_{CEO} \geq 20 \text{ Volts}$$

Fabrication yield in percent						
Bulk material resistivity (ohm-cm)	Emitter junction depth (μ inches)					
	20	25	30	35	40	45
0.5	0	0	0	0	0	0
1.0	45	23	5	1	0	0
1.5	99	75	40	11	0	0
2.0	100	84	45	11	0	0
2.5	100	83	44	9	0	0
	Emitter junction depth (μ inches)					
	20	22	24	26	28	30
1.25	88	77	68	51	36	18
1.5	99	93	83	72	59	40
1.75	100	98	98	77	64	45
2.0	100	98	90	79	64	45
2.25	100	98	91	77	64	44

Table 11 Design-center characteristics—narrow base transistor.

Emitter junction depth	20 (μ inches)
Bulk material resistivity	1.75 (ohm-cm)
Physical base width	20 (μ inches)
Electrical base width	10.3 (μ inches)
Emitter junction capacitance	0.61 (pF/mil ²)
Collector junction capacitance	0.10 (pF/mil ²)
Collector punch-through	146 (volts)
Emitter punch-through	6.7 (volts)
Emitter injection efficiency	6876
Base region transport efficiency	217
Current gain	210
Open-base breakdown	29.5 (volts)

through voltage and reduces the variability of this transistor parameter. In Table 10, for example, a continuous decrease in the percentage of satisfactory transistors, with an increase in emitter junction depth, results from interaction mechanisms between a reduced collector punch-through voltage and the open-base breakdown voltage. Further, a decrease in the bulk material resistivity also reduces the open-base breakdown voltage by increasing carrier multiplication within the collector junction space-charge layer.

After selecting a satisfactory range of emitter junction depths, and bulk material resistivities (Table 10), a more detailed calculation provides the necessary design information. From the lower design matrix in Table 10 it is seen that $x_{je} = 20 \mu$ inches and a bulk material resistivity of 1.75 ohm-cm represents a satisfactory location. This design is not intended to imply that such a structure would be easy to fabricate—it only establishes a means of satisfying the imposed parameter specifications with the assumed base width and diffusion process restrictions. Table 11 presents the design-center parameters of such a device. Although parameter specifications have required $BV_{CEO} \geq 20$ volts, a large variability in the collector punch-through voltage implies the need of a design-center punch-through voltage of 146 volts.

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